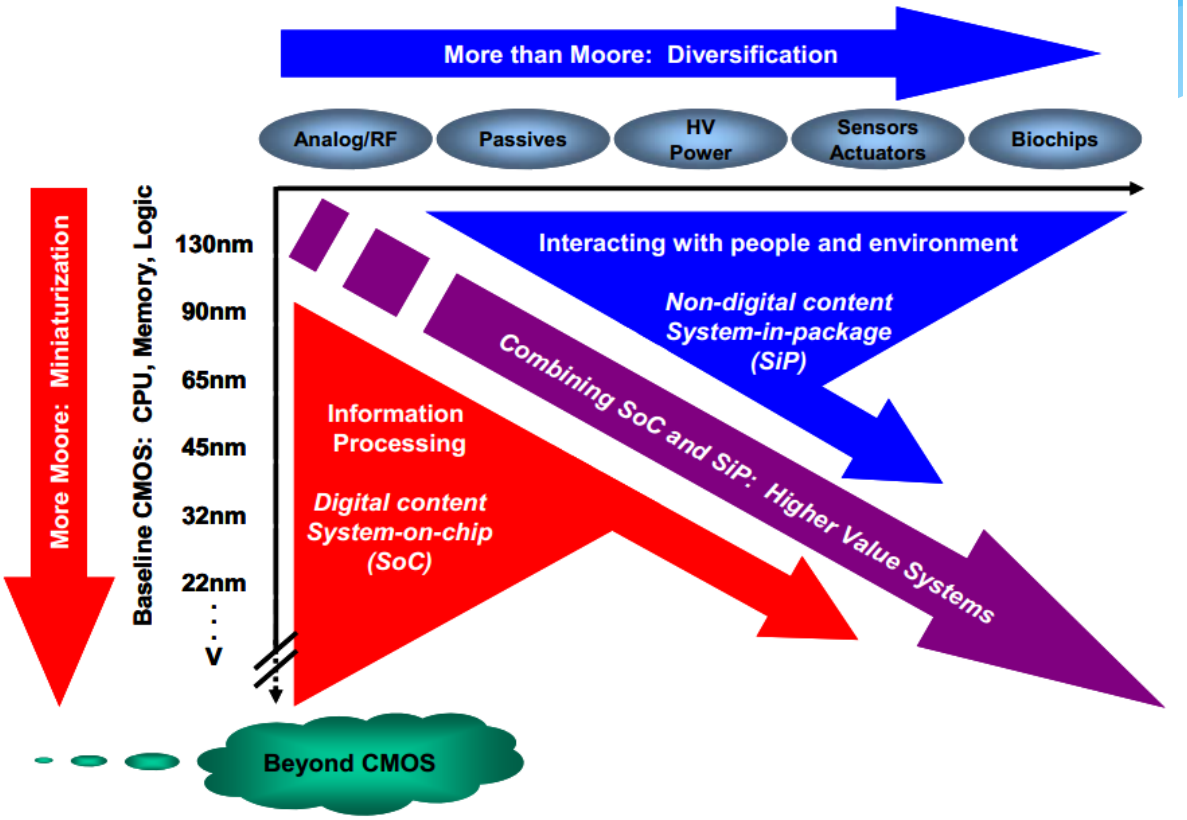
# Modelling and Design of A 45nm SLC 3D NAND Flash CPLD

Arijit Banerjee and Sergiu Mosanu

Date: 5/15/2015

# End of Moore's Law and Future Technologies

- Device scaling has reached molecular dimensions
- 2D Moore's law is about to end
- 3D can be an option to further device scaling




Courtesy: ITRS 2012

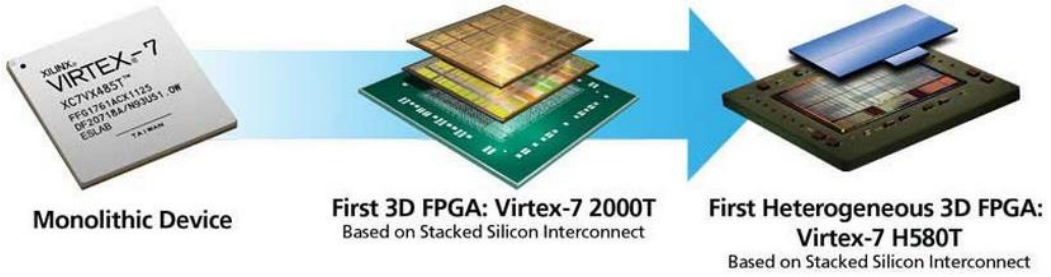
# 3D IC: Adding a New Dimension

- Higher density
- Faster clock rates
- Lower in power
- 3D using stacked silicon die connected using through silicon via (TSV)s
- 2.5D using silicon interposers
- 2.5D using heterogeneous die packaging
- Monolithic 3D ICs: 3D NAND flash


Courtesy: Yole Report 2007, and IEEE

# 3D FPGA

* Benefits
  * Higher density
  * Faster clock rates
  * Lower in power
  * Flexibility
  * Re-configurability
  * Lower cost for prototyping
* Combining monolithic 3D NAND flash in complex programmable logic device (CPLD) or FPGAs could drastically improve literal or logic density



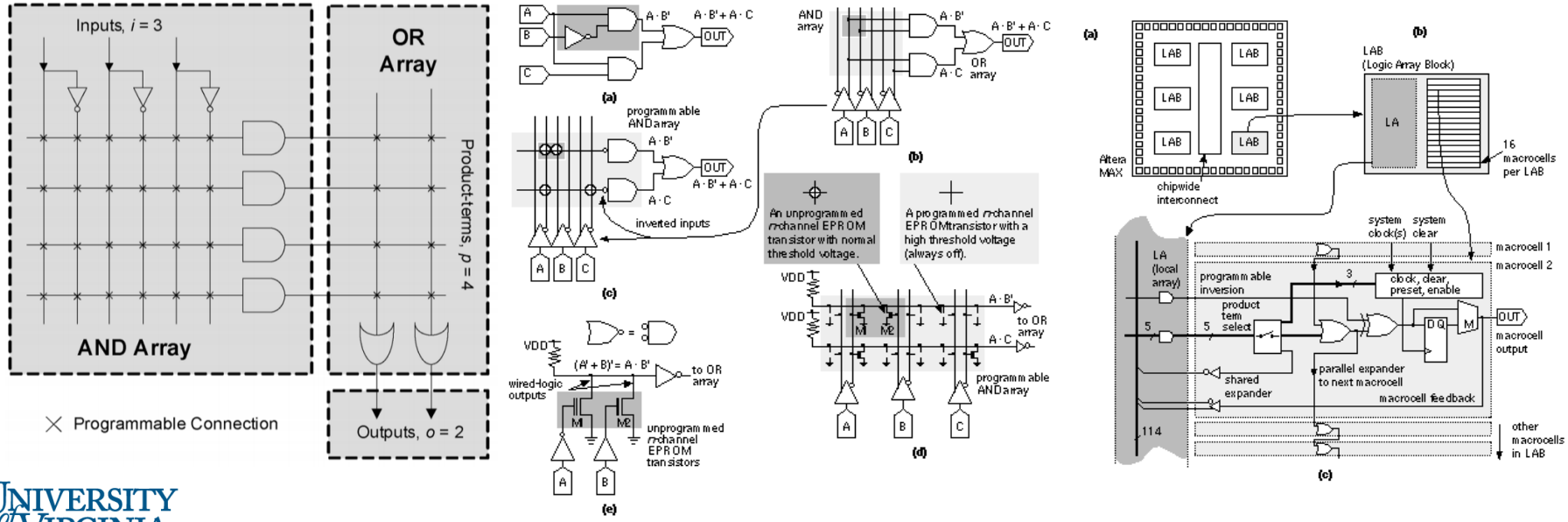

Courtesy: Xilinx.com

# Outline

* Revisiting Complex programmable logic devices (CPLD)
* Modelling SLC NAND bitcell
* SLC NAND planes in 3D CPLDs
* 3D NAND array write, read and erase operations
* Circuit design for write, read and erase operations
* 3D configurable logic block (CLB) architecture
* 3D CPLD and FPGA architecture
* PPA of the CLB
* 3D NAND array physical design and visualization

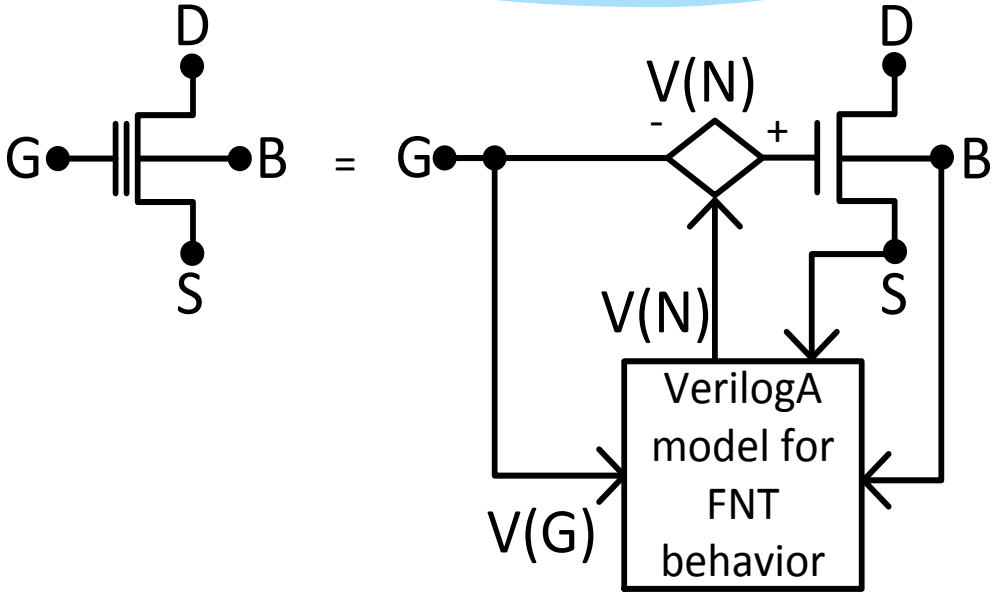
# Revisiting Complex Programmable Logic Devices (CPLD)

* CPLDs used for gluing multiple chips to interact
* Two programmable PLA planes for complex programming
* The programmable planes can be replaced with two 3D NAND flash planes to achieve higher logic density



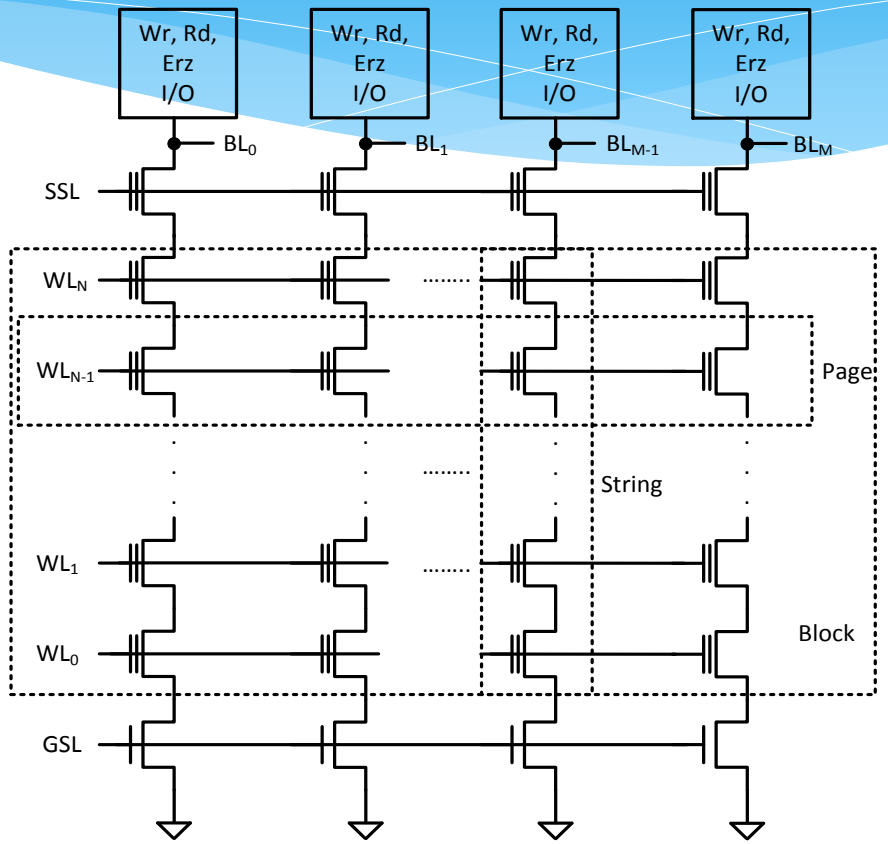
# Modelling an SLC NAND Bitcell in SPICE and Veriloga

- SLC bitcell has two states: 1 and 0 logically
- Behaviorally modelled the FNT behavior for SLC bitcell write and erase operation using a Veriloga model, a VCVS and a HVT NMOS
- Veriloga model senses the gate, source and body potential of the NMOS to generate a VCVS as V(N) that exactly mimics the storage bits, write and erase operation for SLC bitcell



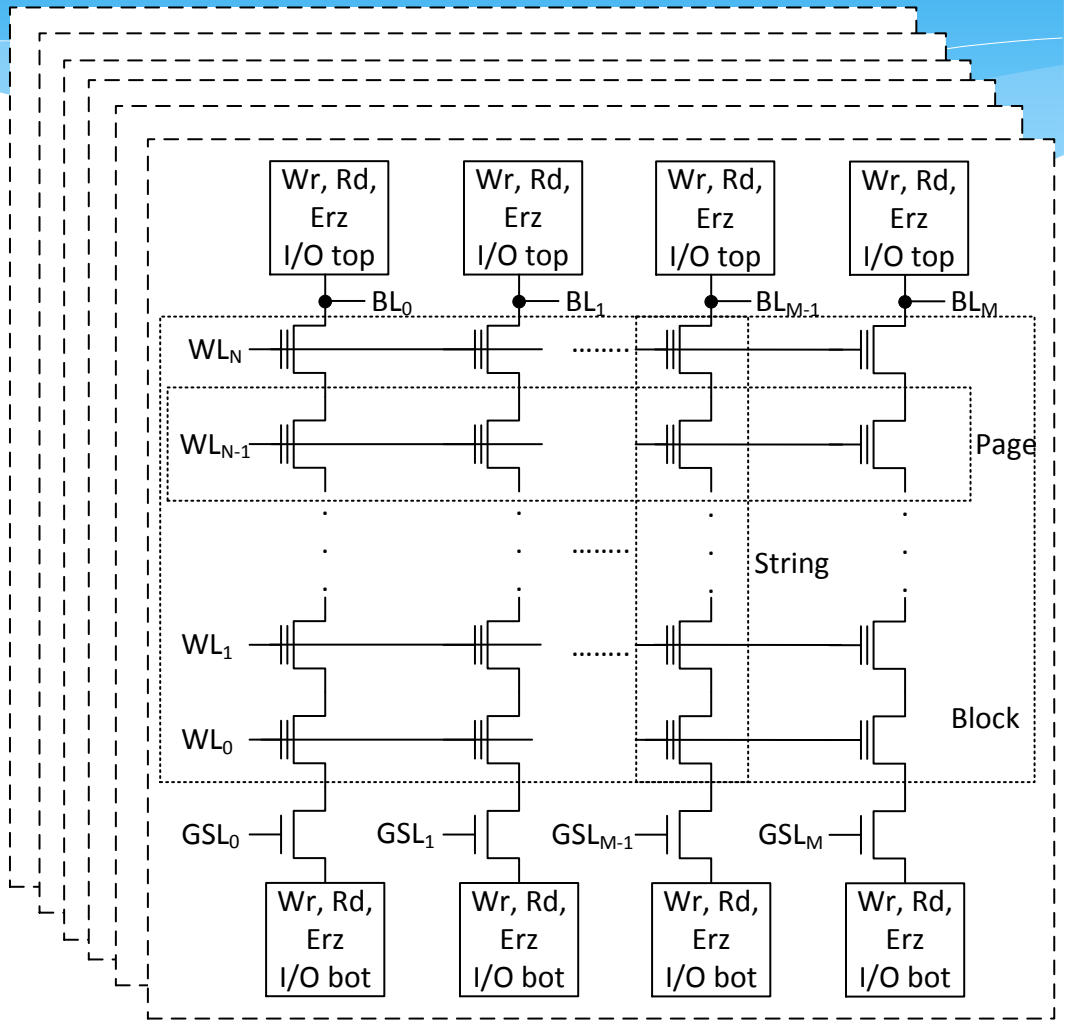
# Typical NAND Flash Array

* As string is associated with a single bitline for write and read operation
* The bitcells in the same page has the same wordline
* Multiple pages forms a block or array which can be erased at the same time

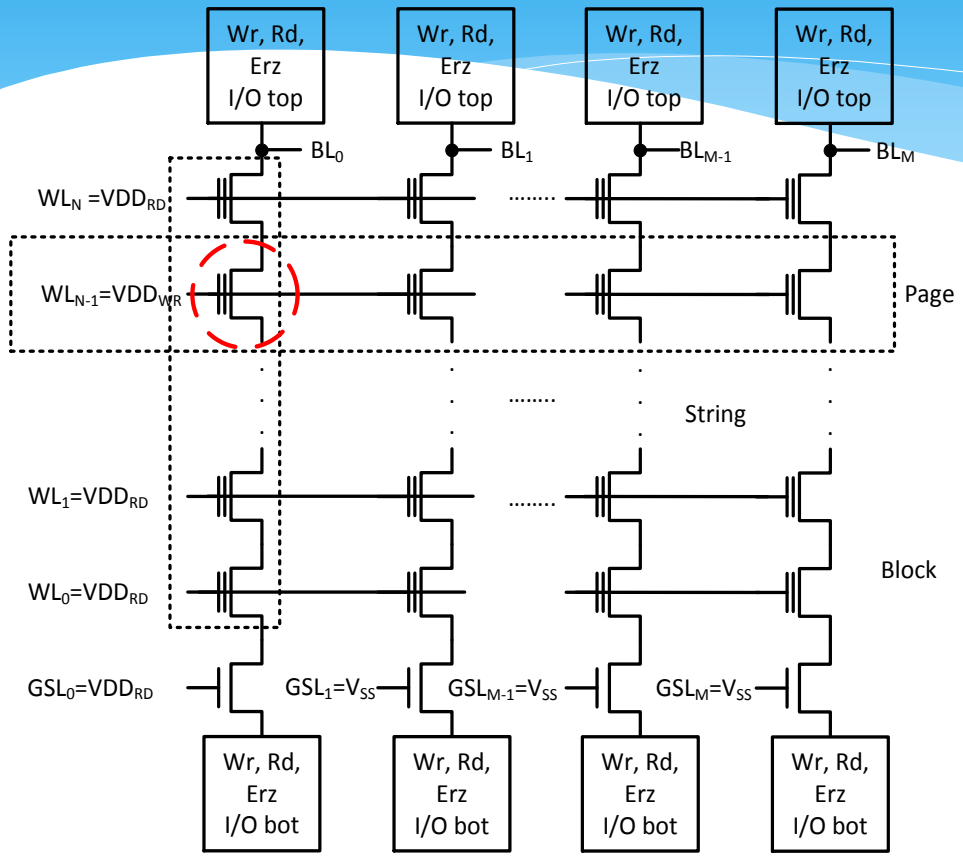


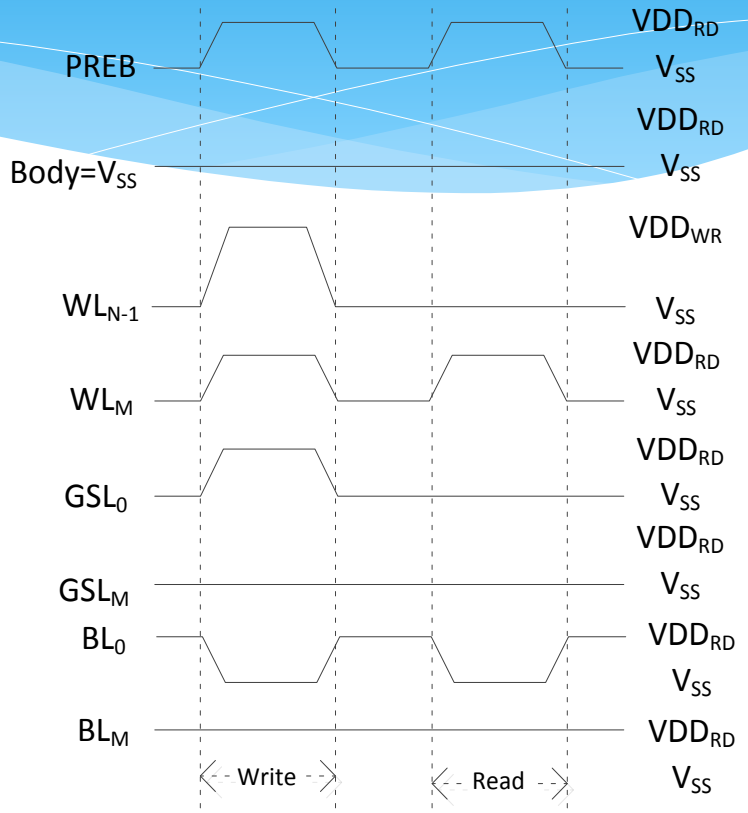
# SLC NAND Planes in 3D CPLDs

- Each string is of 16 SLC bitcell
- Each page in two NAND planes has 16 SLC bitcell per CLB in a distributed architecture
- Right figure shows a centralized 3D NAND architecture
- GSL lines are controlled inside the Bot I/O, but shown individually for simplicity



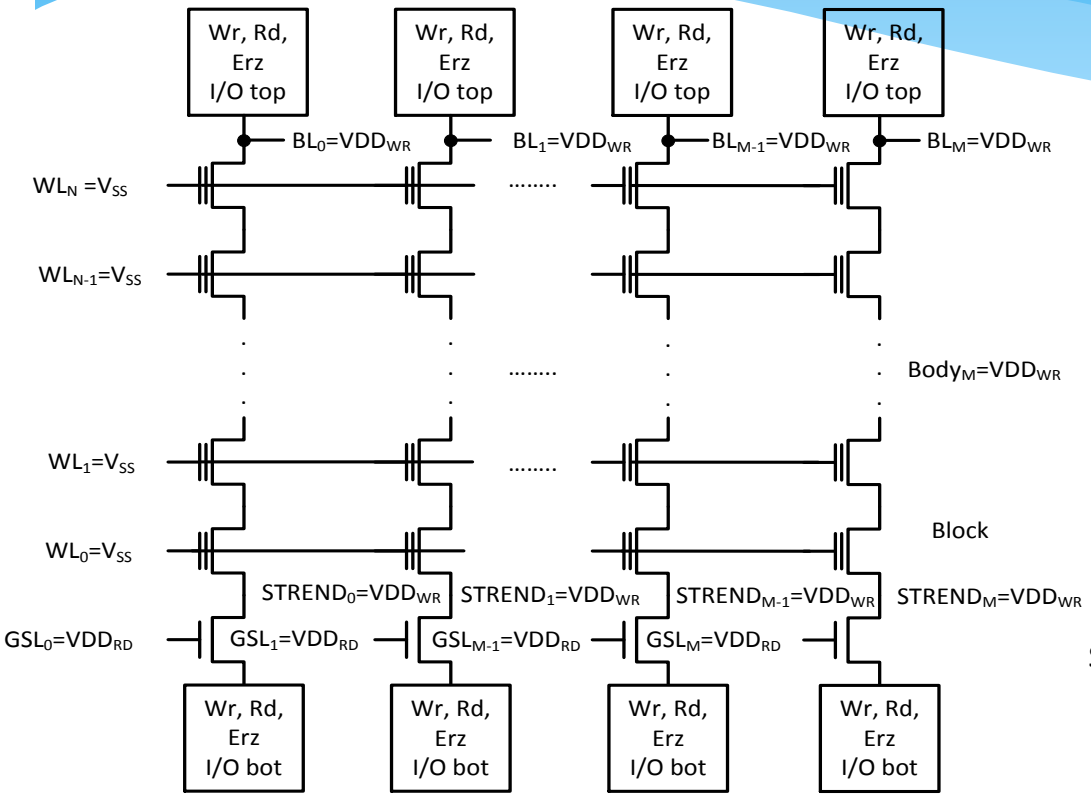
# Ideal Write and Read Operation in SLC 3D NAND Planes

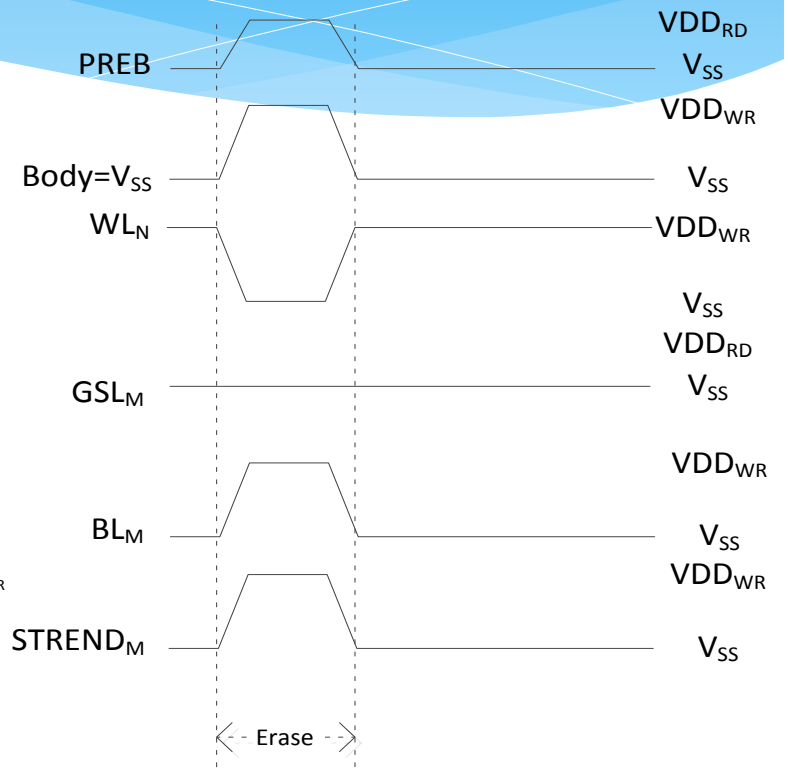



NAND Flash Write and Read Operation

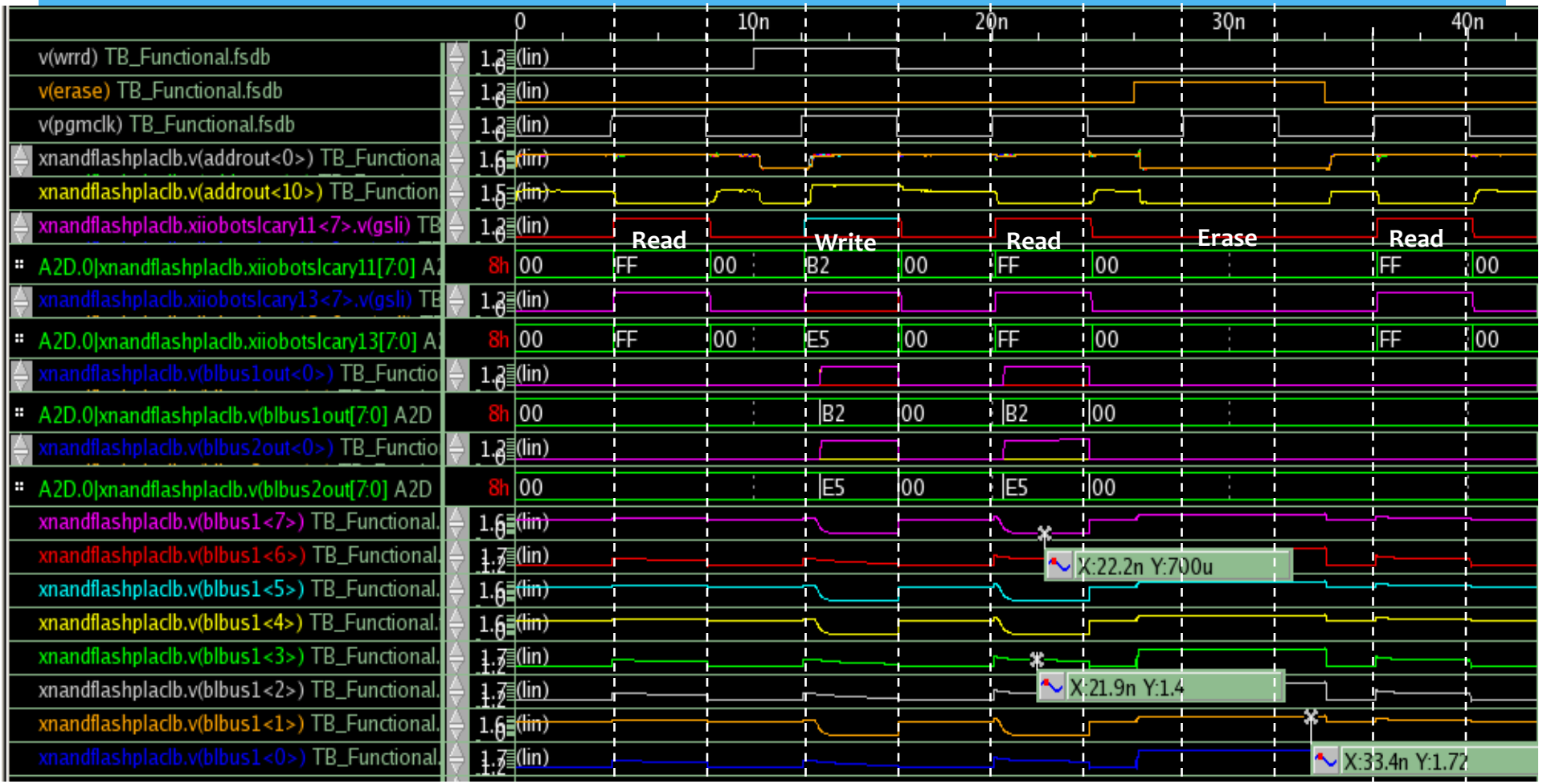
# Ideal Erase Operation in SLC 3D NAND Planes



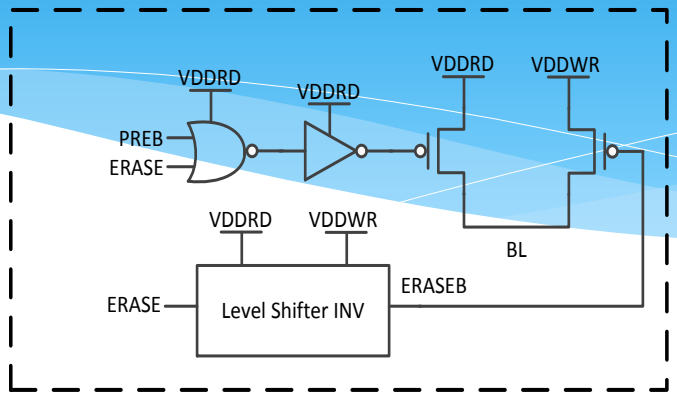

NAND Flash Erase Operation

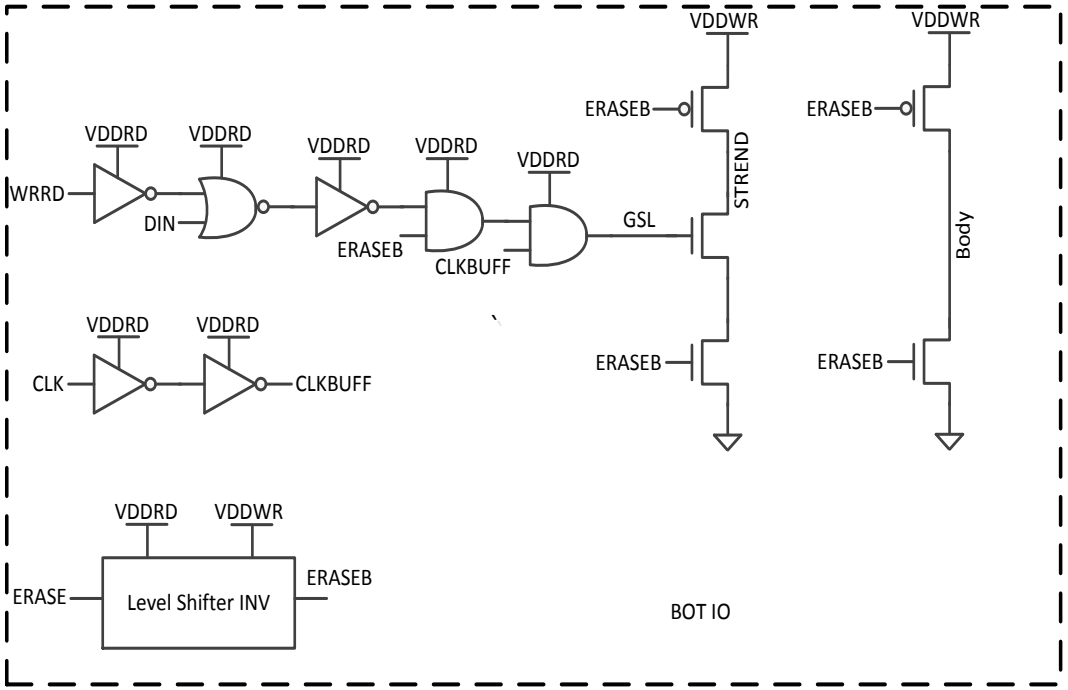
# Actual Energy Efficient Write Read and Erase Waveforms @ 125MHz



# Top and Bottom I/O for Write, Read and Erase Operations for SLC 3D NANAD Array

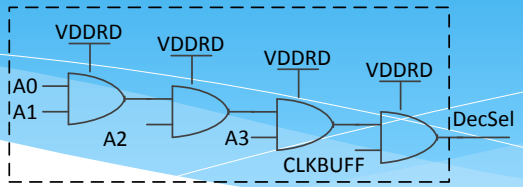
- Top and Bot I/O generate the write, read and erase voltages
- They also generate write waveforms as per the data in Bot I/O



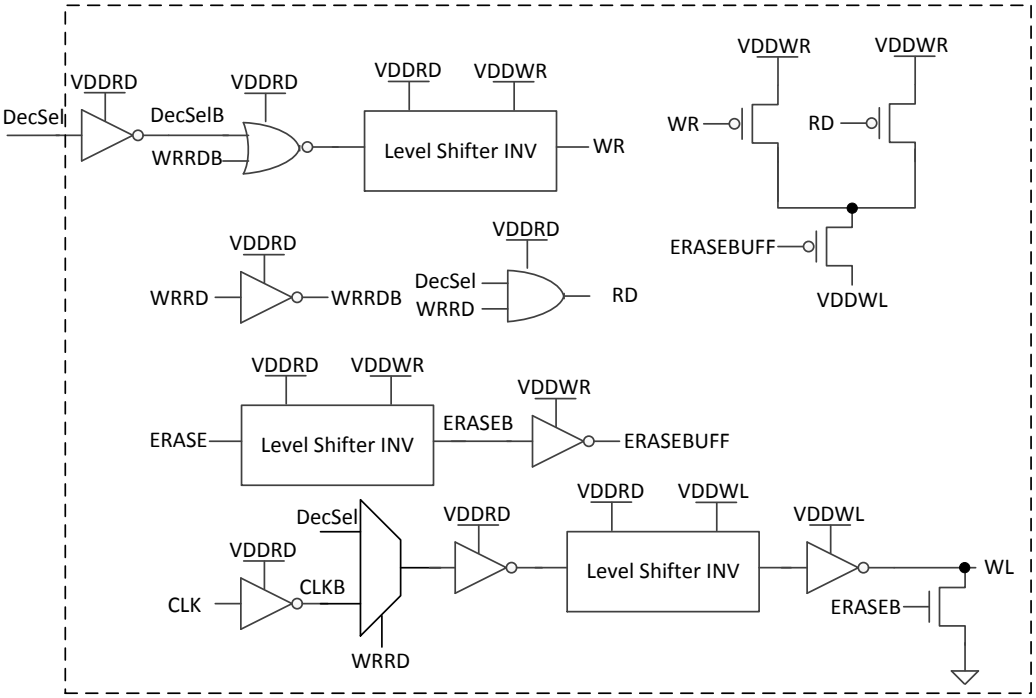



# Wordline Driver for Write, Read and Erase Operations for SLC 3D NANAD Array

- Wordline driver generates all the necessary voltages for write, read and erase operation
- Uses level converters and PMOS switches to change supply voltages

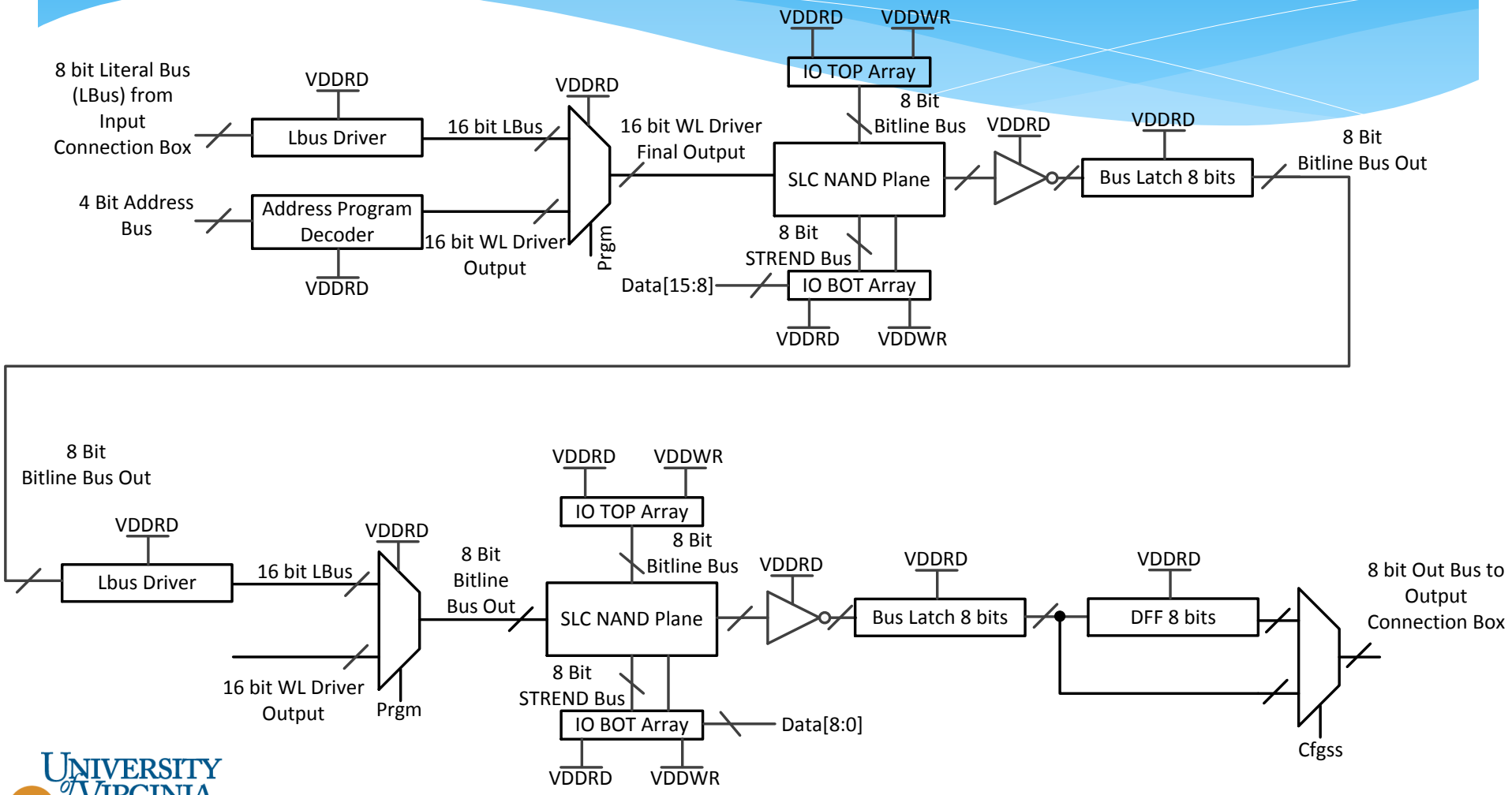



Decoder slices



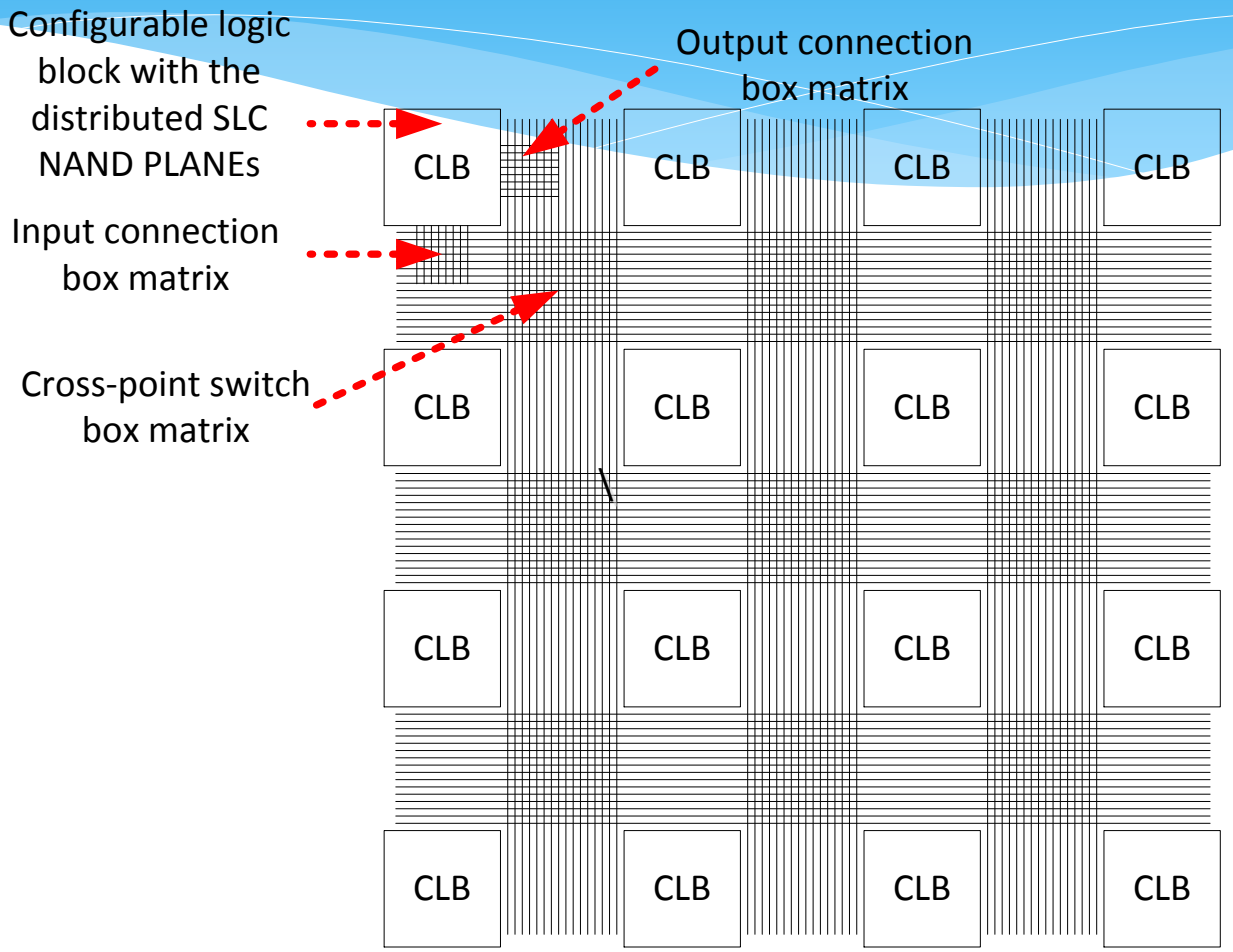

Wordline driver slices

# 3D Configurable Logic Block Architecture for CPLD and FPGAs



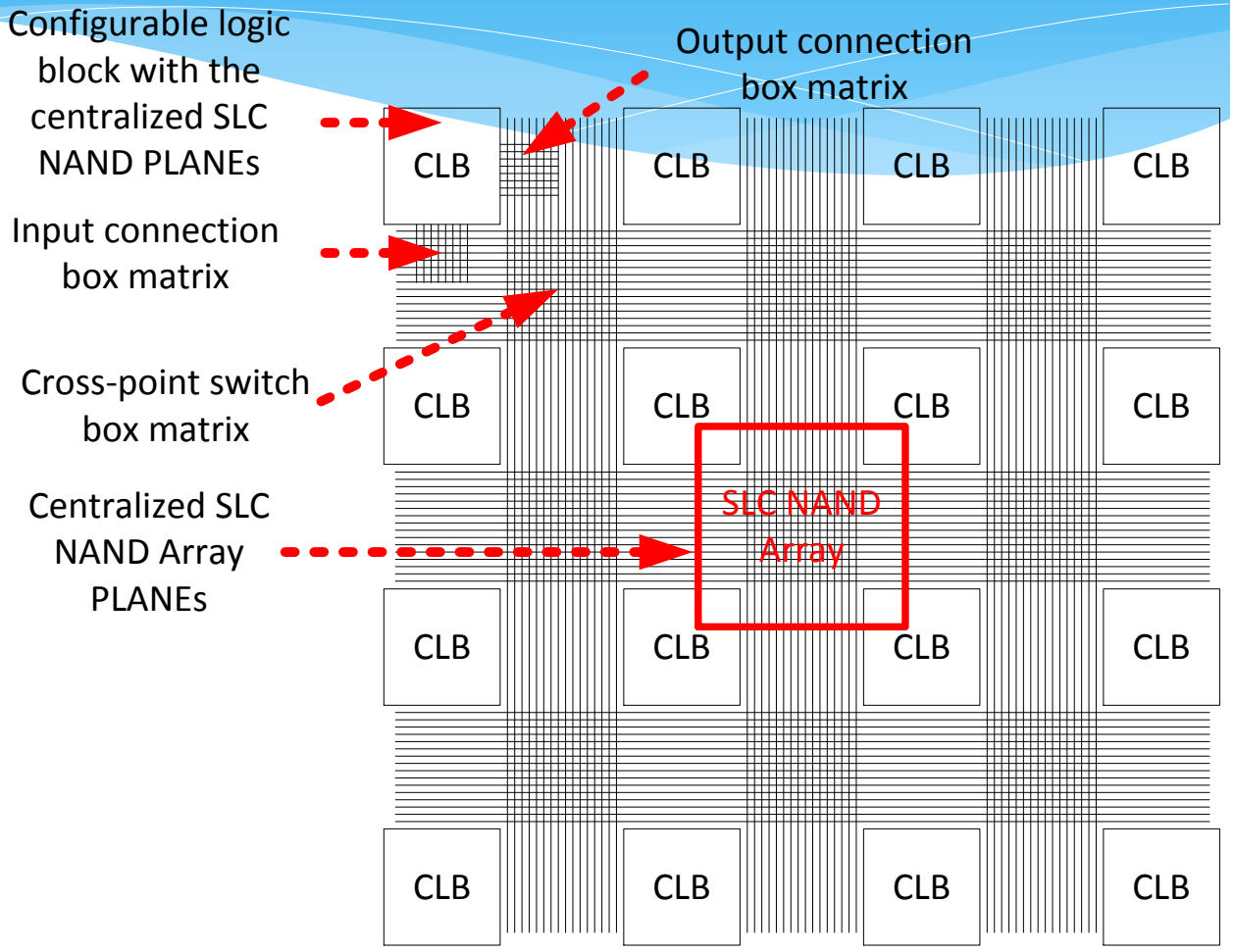
# Distributed 3D NAND architecture for 3D CPLD and FPGAs

- CLB contains the 16X8 two 3D NAND planes
- Routing cost is minimal for WL and BL routability
- There can be mask cost overhead for the 3D NAND planes
- There can be structural brittleness in the 3D NANDs with only two planes per CLB



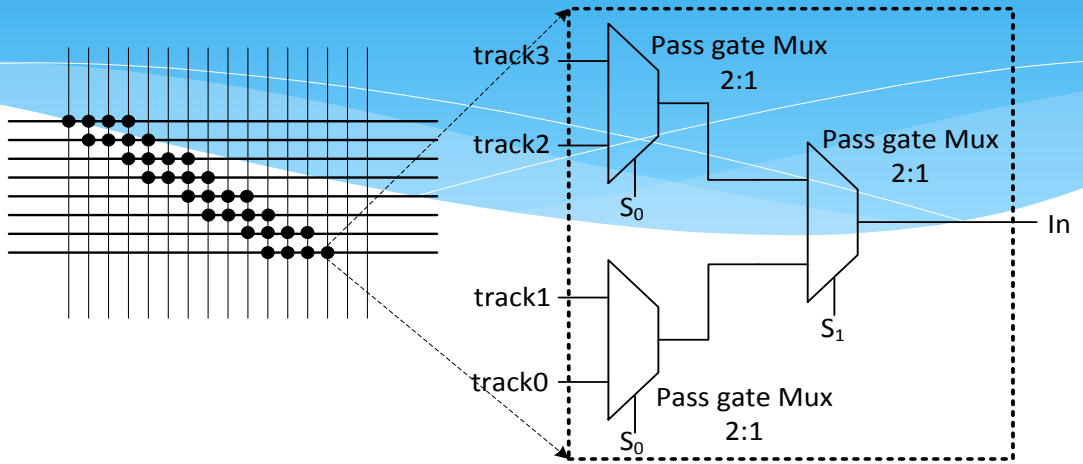
# Centralized 3D NAND architecture for 3D CPLD and FPGAs

- CLB contains no 3D NAND planes: all the NAND planes are centralized in the middle of the CPLD as a cluster
- Routing cost is higher for WL and BL routability and may need extra area or metal options
- The mask cost overhead for the 3D NAND planes is less as it is centralized
- Structurally, it is less brittle in the 3D NAND centralize array planes

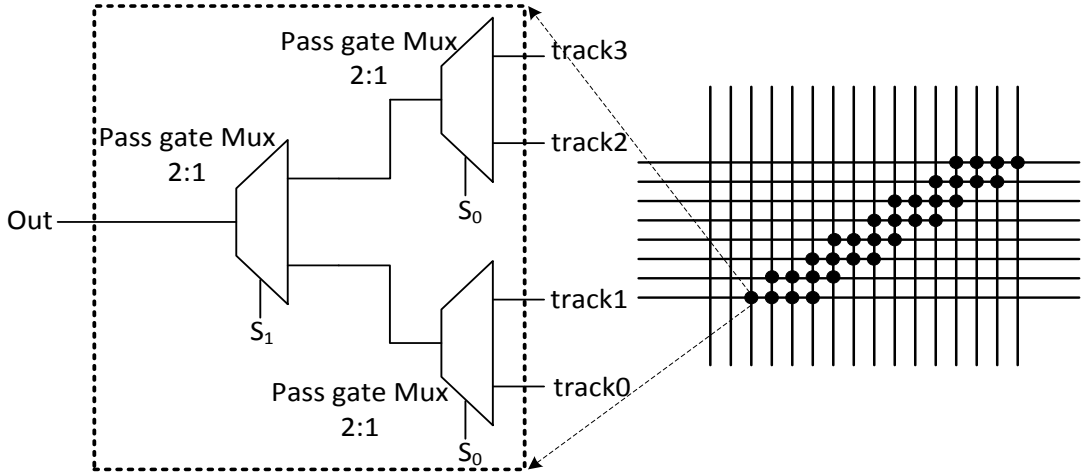


# Input and Output Connection Boxes for 3D CPLD and FPGAs

* Used flexibility of 4 overlapping connection topology for Input and output connection boxes
* Muxes are PMOS-NMOS transmission gate mux for passing the true logic levels
* Total of 8X4=32 programmable connection per connection box to the CLBs



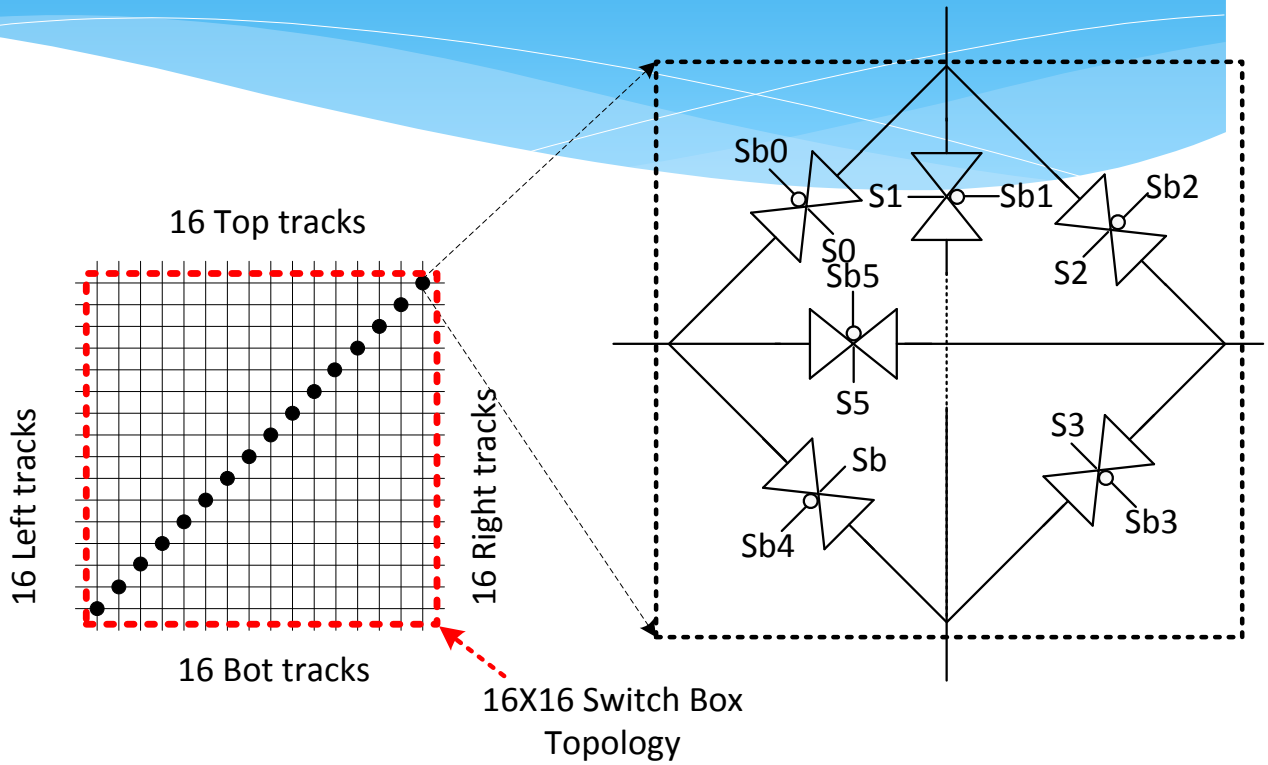

(a) Input connection box and switch




(b) Output connection box and switch

# Switch Box Architecture for 3D CPLD and FPGAs

* Switch box topology is simpler than the Planer and Wilton topology
* Uses diagonal connections in the connection matrix
* This topology makes the track lengths as 1 unit
* Connections are made using transmission gate logic that uses distributed SRAMs to be programmed



# PPA of 3D CPLD or FPGAs using monolithic 3D NAND Flash Technology

- Area per literal is 10X smaller using 3D NAND structures in monolithic 3D FLASH CPLDs than planer NAND CPLDs
- Read, write and erase can be done up to 499MHz clock rate
- Power numbers are also reasonable

| Speed Max | Read Power/Literal (mW) | Write Power/Literal (mW) | Erase Power (mW) |
|---|---|---|---|
| 495MHz | 51.53 | 44.65 | 66.49 |

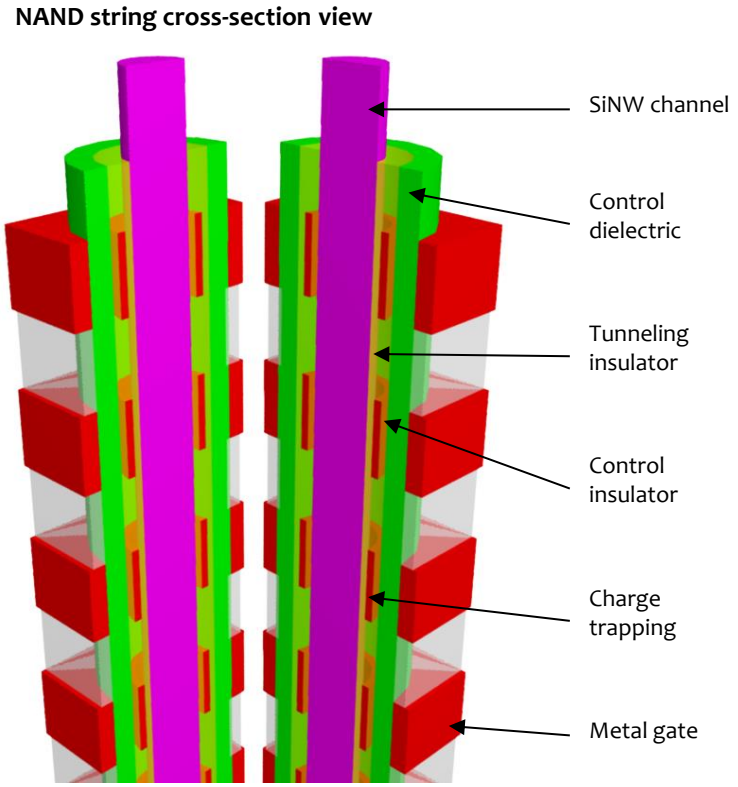
| | SLC Planer NAND in CPLDs | SLC 3D NAND in CPLDs | Area Improvement |
|---|---|---|---|
| Area/Literal ($\mu^2$ / literal) | 0.48 | 0.045 | ~10X |

# Visualization and design in 3D

* Using of Autodesk Maya
* Maya Embedded Language (MEL) script

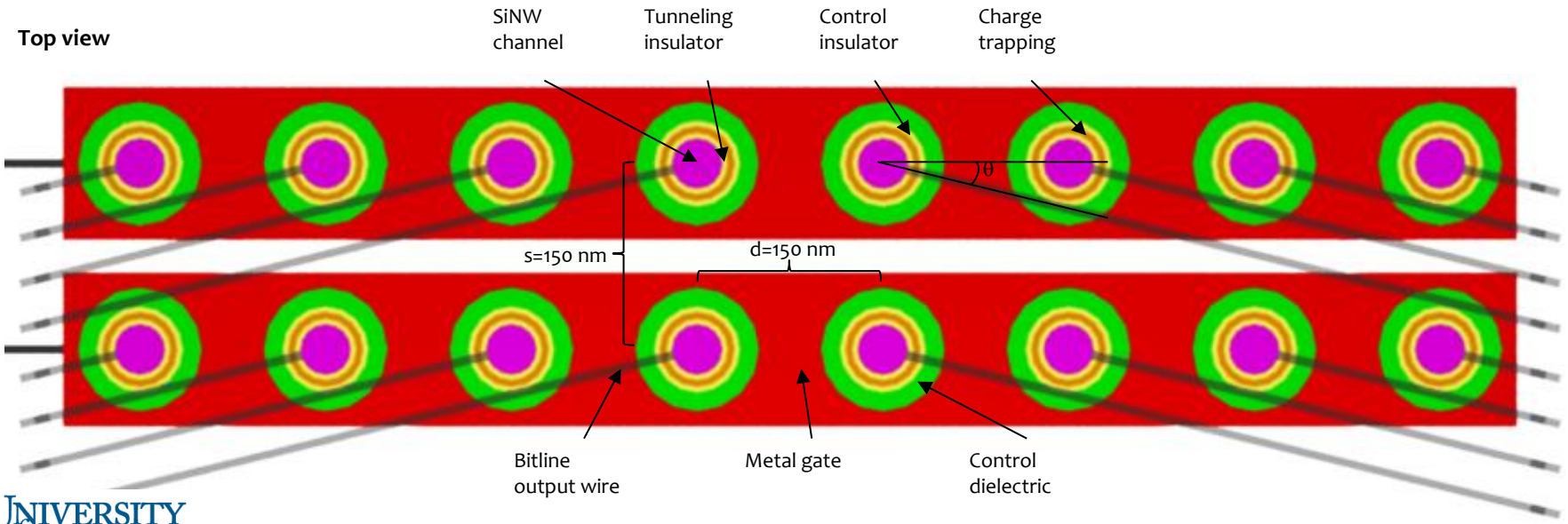
# NAND string layer structure

* Cylinder/pipe layer structure
* SiNW channel
* Insulator layer
* Charge trapping all-around metal floating gates
* Dielectric layer
* Tunneling and control
* All-around metal gates



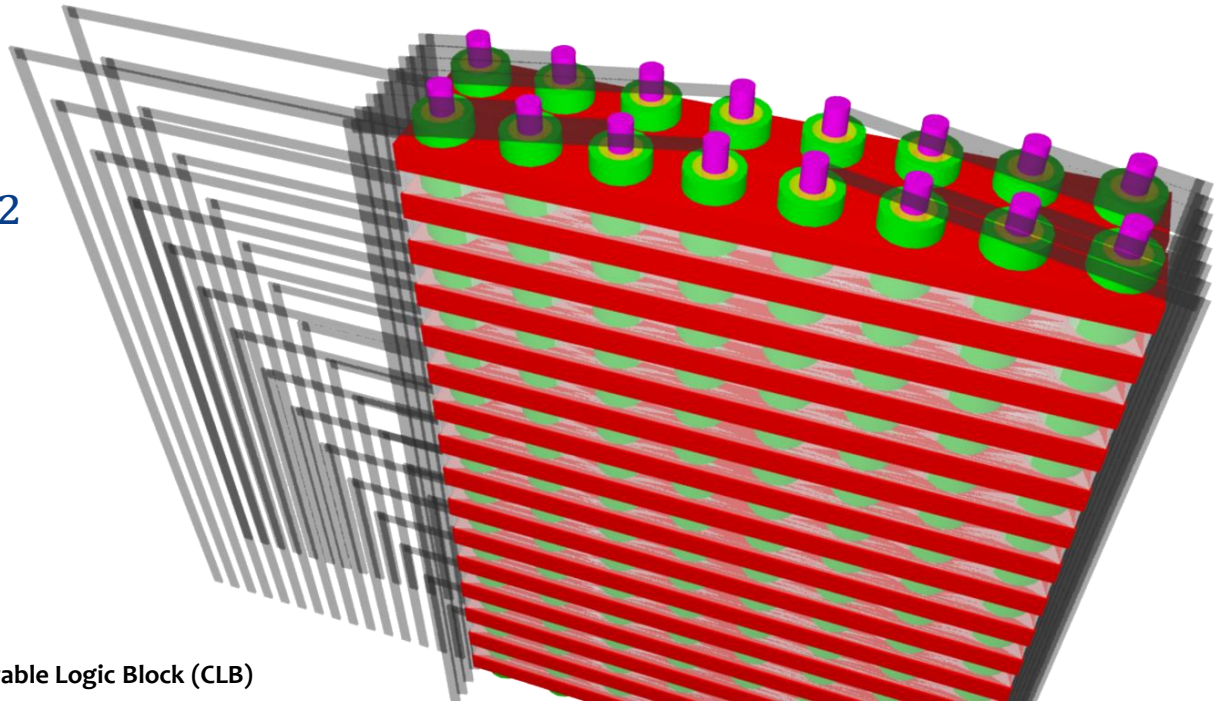
# Bitline and wordline wiring

* Each bitline/wordline wired to mainboard
* Equal NAND string & plane spacing
* Bitlines on top, at an angle θ
* $\tan^{-1}\frac{r_{channel}+space}{d} < \theta < \tan^{-1}\frac{s-(r_{channel}+space)}{3\cdot d}$



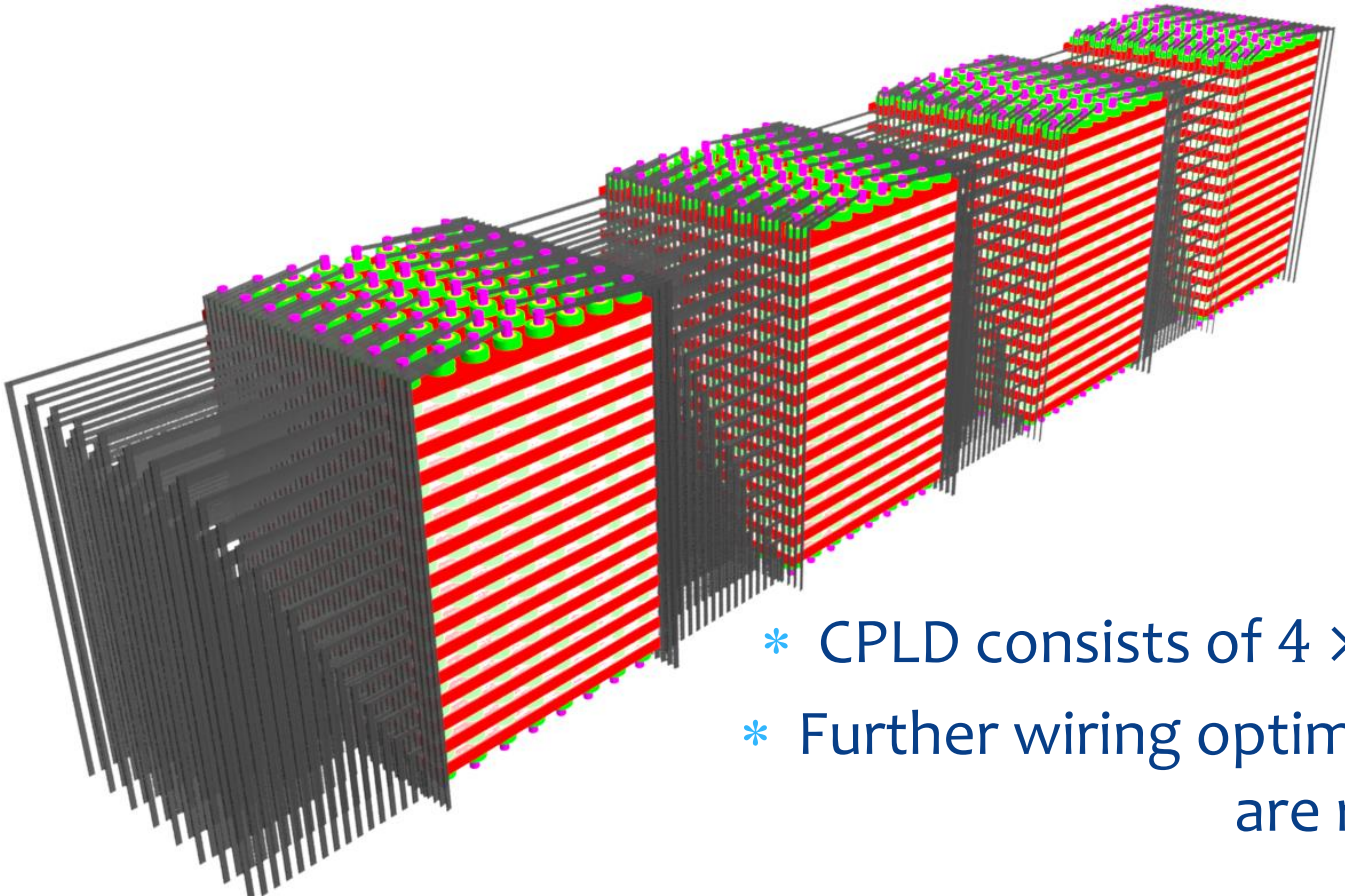
# Distributed 3D NAND planes in a CLB to full CPLD

* 8 NAND strings in a row form a $8 \times 16$ NAND plane
* 2 NAND planes form a CLB containing 256 3D NAND FGMOS
* CLB area: $0.36\mu m^2$
* NAND String area:
  * $0.0225\mu m^2$
* Area/literal: $0.045\mu m^2$
* Footprint with wires:
  * $0.6\mu m^2$
  * $0.075\mu m^2$/literal



Configurable Logic Block (CLB)

# Centralized 3D NAND Buildings in a Full CPLD



* CPLD consists of 4 × 4 CLBs
* Further wiring optimizations are required

UNIVERSITY of VIRGINIA ENGINEERING

# Conclusions

* 3D Flash technology in CPLD and FPGAs can provide high literal density with the support of complex Boolean functions
* Programming and block erase speed is higher
* Programming power consumption per literal is less than 100mW at 495MHz
* Suffers from required read latching of data in the CLB even when the implementation is combinatorial

# References


* [1] Moon, J.S.; Curtis, D.; Hu, M.; Bui, S.; Wheeler, D.; Marshall, T.; Sharifi, H.; Wong, D.; Gaskill, D.K.; Campbell, P.M.; Asbeck, P.; Jernigan, G.; Tedesco, J.; VanMil, B.; Myers-Ward, R.; Eddy, C.; Weng, X.; Robinson, J.; Fanton, M., "Self-aligned graphene-on-SiC and graphene-on-Si MOSFETs on 75 mm wafers," *Device Research Conference (DRC), 2010* , vol., no., pp.209,210, 21-23 June 2010.
* [2] Junho Cheon; Seongwook Choi; Young Jun Heo; Seok Ha Lee; Jaeheung Lim; Young June Park, "Fabrication of n-Type CNT Field-Effect Transistor Using Energy Band Engineering Layer Between CNT and Electrode," *Electron Device Letters, IEEE* , vol.34, no.11, pp.1436,1438, Nov. 2013.
* [3] del Alamo, J.A., "InGaAs nanoelectronics: from THz to CMOS," *Electron Devices and Solid-State Circuits (EDSSC), 2013 IEEE International Conference of* , vol., no., pp.1,1, 3-5 June 2013.
* [4] Mishra, A.; Pattanaik, M.; Sharma, V., "Double gate vertical tunnel FET for hybrid CMOS-TFET based low standby power logic circuits," *Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), 2013 Annual International Conference on* , vol., no., pp.1,4, 4-6 June 2013.
* [5] Zhenyu Sun; Xiuyuan Bi; Hai Li; Weng-Fai Wong; Xiaochun Zhu, "STT-RAM Cache Hierarchy With Multiretention MTJ Designs," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol.22, no.6, pp.1281,1293, June 2014.
* [6] Kim, H.H.; Song, Y.J.; Lee, S.Y.; Joo, H.J.; Jang, N.W.; Jung, D.J.; Park, Y.S.; Park, S.O.; Lee, K.M.; Joo, S.H.; Lee, S.W.; Nam, S.D.; Kim, K., "Novel integration technologies for highly manufacturable 32 Mb FRAM," *VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on* , vol., no., pp.210,211, 11-13 June 2002.
* [7] Jing Xie; Yu Wang; Yuan Xie, "Yield-aware time-efficient testing and self-fixing design for TSV-based 3D ICs," *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific* , vol., no., pp.738,743, Jan. 30 2012-Feb. 2 2012.
* [8] Palesko, C.; Palesko, A.; Vardaman, E.J., "Cost and yield analysis of multi-die packaging using 2.5D technology compared to fan-out wafer level packaging," *Electronics System-Integration Technology Conference (ESTC), 2014* , vol., no., pp.1,5, 16-18 Sept. 2014.
* [9] Qiao Chen; Suzuki, Y.; Kumar, G.; Sundaram, V.; Tummala, R.R., "Modeling, Fabrication, and Characterization of Low-Cost and High-Performance Polycrystalline Panel-Based Silicon Interposer With Through Vias and Redistribution Layers," *Components, Packaging and Manufacturing Technology, IEEE Transactions on* , vol.4, no.12, pp.2035,2041, Dec. 2014.
* [10] Thomas, O.; Vinet, M.; Rozeau, O.; Batude, P.; Valentian, A., "Compact 6T SRAM cell with robust read/write stabilizing design in 45nm Monolithic 3D IC technology," *IC Design and Technology, 2009. ICICDT '09. IEEE International Conference on* , vol., no., pp.195,198, 18-20 May 2009.
* [11] Panth, S.; Samadi, K.; Yang Du; Sung Kyu Lim, "High-density integration of functional modules using monolithic 3D-IC technology," *Design Automation Conference (ASP-DAC), 2013 18th Asia and South Pacific* , vol., no., pp.681,686, 22-25 Jan. 2013.
* [12] Chang-Hong Shen; Jia-Min Shieh; Tsung-Ta Wu; Wen-Hsien Huang; Chih-Chao Yang; Chih-Jen Wan; Chein-Din Lin; Hsing-Hsiang Wang; Bo-Yuan Chen; Guo-Wei Huang; Yu-Chung Lien; Wong, S.; Chieh Wang; Yin-Chieh Lai; Chien-Fu Chen; Meng-Fan Chang; Chenming Hu; Fu-Liang Yang, "Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM," *Electron Devices Meeting (IEDM), 2013 IEEE International* , vol., no., pp.9.3.1,9.3.4, 9-11 Dec. 2013.
* [13] J.H. Lee et al., "Three-dimensional NAND Flash architecture design based on single-crystalline STacked ARray" in *IEEE Transactions on electron devices,* Vol. 59, No. 1, January 2012.
* [14] B. Prince, "Vertical 3D memory technologies", John Wiley and Sons Ltd 2014.
* [15] K.T. Park, et al. "Three-dimensional 128 Gb MLC vertical NAND Flash memory with 24-WL stacked layers and 50 MB/s high-speed programming", in *IEEE journal of solid-state circuits, Vol. 50, No. 1 January 2015.*
* [16] Furuta, F.; Matsumura, T.; Osada, K.; Aoki, M.; Hozawa, K.; Takeda, K.; Miyamoto, N., "Scalable 3D-FPGA using wafer-to-wafer TSV interconnect of 15 Tbps/W, 3.3 Tbps/mm$^2$," *VLSI Circuits (VLSIC), 2013 Symposium on* , vol., no., pp.C24,C25, 12-14 June 2013.
* [17] Wolf, M.J.; Ramm, P.; Klumpp, A.; Reichl, H., "Technologies for 3D wafer level heterogeneous integration," *Design, Test, Integration and Packaging of MEMS/MOEMS, 2008. MEMS/MOEMS 2008. Symposium on* , vol., no., pp.123,126, 9-11 April 2008.
* [18] Vaughn Betz , Jonathan Rose , Alexander Marquardt, "Architecture and CAD for Deep-Submicron FPGAs," Kluwer Academic Publishers, Norwell, MA, 1999.
* [19] Soofiani, J.S.; Masoumi, N., "Area efficient switch box topologies for 3D FPGAs," *New Circuits and Systems Conference (NEWCAS), 2011 IEEE 9th International* , vol., no., pp.390,393, 26-29 June 2011.


UNIVERSITY of VIRGINIA ENGINEERING

# Questions

**THANK YOU!**

**GO HOOS!**

UNIVERSITY of VIRGINIA ENGINEERING